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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,542	11/13/2001	Chan Yong Lee	8750-19	3270

7590

07/23/2002

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EXAMINER

LE, THONG QUOC

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 07/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Appli cation No.

10/002,542

Applicant(s)

LEE ET AL.

Examiner

Thong Q. Le

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 6. 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-15 in Paper No. 7 is acknowledged.
2. **A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.**
3. Claims 1-15 are presented for examination.

Information Disclosure Statement

4. This office acknowledges receipt of the following items from the Applicant:
Information Disclosure Statement (IDS) filed on November 13, 2001.
Information Disclosure Statement (IDS) filed on June 03, 2002.
5. Information disclosed and list on PTO 1449 was considered.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7. Claims 2-14 are objected to because of the following informalities:
Regarding claims 2-14, line 1, should be change "A circuit" to – The circuit--.

8. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

10. Claims 1-3, 7-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claims 1-3, Figure 5 of AAPA is directed to a circuit comprising: a read charge control circuit (PSA) activated by a read signal (SCL) and an address; and a write charge control circuit (DIOG3) activate by a write signal (WR) and the same or different address, the read charge control circuit and the write charge control circuit both coupled to common data IO lines (DIO, DIOB), and the read charge control circuit is a sense amplifier (10), and the write charge control circuit transfers charge between the data IO lines and bit lines (DIO and DIOB transfers charge to bit lines by N7 and N8, N15, N16).

Regarding claims 7-9, AAPA discloses the read charge control circuit including a first read controlled gate charge from the bit line to a complimentary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line (N7, N8), and the first and second read controlled gates are controlled by a read column select line signal (CSL).

Regarding claims 10-11 AAPA discloses a data output sense amplifier coupled between a data output buffer and the data IO lines (DATA OUTPUT SENSE AMPLIFIER), and including load transistors shared between the read a data output buffer (20) and the data output sense amplifier (L1, L2).

Regarding claims 12-14, and 15, AAPA discloses the read charge control circuit includes a first transistor (N7) having a first terminal coupled to a bit line, a second control terminal coupled to a complementary data IO line and a third terminal, a second transistor (N8) having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal, and a third transistor having a first coupled to (N6) a column select line (CSL), a second terminal coupled to the third terminal of the first and a second transistor and a third terminal coupled to a first reference voltage VSS, and the write charge control circuit includes a first transistor (N12) having a first terminal coupled to a write column select line (WR), a second terminal coupled to the complementary line bit line and a third terminal coupled to the complementary data IO line; and a second transistor (N13) having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line, and a first load transistor (L1) having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage, and a second load transistor (L2) having a first terminal coupled to the second reference voltage, a second terminal coupled to the complement data IO line and a third terminal coupled to the third reference voltage.

Claim Rejections - 35 USC § 103

11. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over in Figure 5 in AAPA, and further in view of Figure 3 in AAPA.

Figure 5 in AAPA as described above, fails to disclose the write charge control circuit has only two write control transistors. However, in Figure 3 in AAPA discloses a write charge control circuit DIOG2 has two write transistors (N9, N10) connected to data IO lines and bit lines and controlled by a write column select line signal (WCSL) to write data into select memory cell in column. Therefore, it would have been obvious to one ordinary skill in the art to use a write charge control circuit has two transistors or four transistors to control select memory column.

Therefore, it would have been obvious to a person of ordinary skill in this art to modify write charge control in Figure 3 in to Figure 5 to obtain the invention as specified in claims 4-6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 703-306-9123. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

A handwritten signature in black ink, appearing to read 'Thong Q. Le'.

Thong Q. Le
Examiner
Art Unit 2818

July 18, 2002